

SPICE Device Model Si3430DY Vishay Siliconix

N-Channel 100-V (D-S) MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

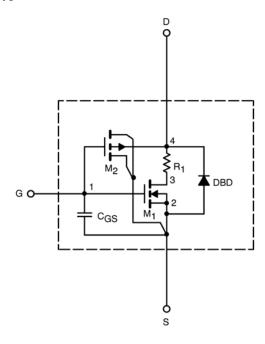
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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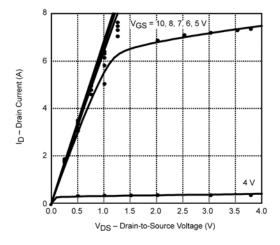
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Conditions	Typical	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS}$ = 10 V	34	А
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 2.4 A	0.146	Ω
		V _{GS} = 6 V, I _D = 2.3 A	0.154	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 2.4 A	8.1	S
Diode Forward Voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	0.72	V
Dynamic ^b				
Total Gate Charge ^b	Q_{g}	V_{DS} = 50 V, V_{GS} = 10 V, I_{D} = 2.4 A	6.06	nC
Gate-Source Charge ^b	Q_{gs}		1.5	
Gate-Drain Charge ^b	Q_{gd}		1.4	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = 50 \text{ V}, R_L = 50 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$ $I_F = 1.7 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	8	ns
Rise Time ^b	t _r		10	
Turn-Off Delay Time ^b	$t_{d(off)}$		23	
Fall Time ^b	t _f		30	
Source-Drain Reverse Recovery Time	t _{rr}		52	

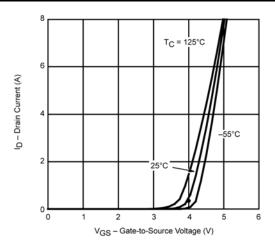
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2% b. Guaranteed by design, not subject to production testing.

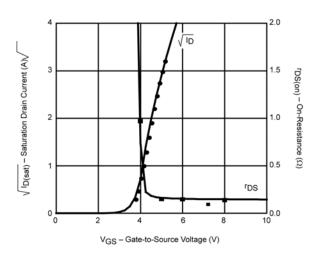


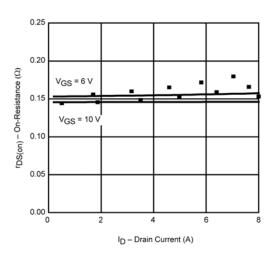
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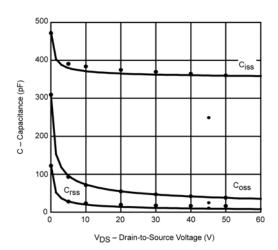
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

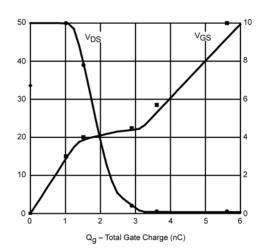












Note: Dots and squares represent measured data.



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Document Number: 91000 Revision: 18-Jul-08

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